## REMARKS

Claims 1-5 are of record. A new claim 6 has been added.

Figs. 7 and 8 have been amended to show the designation PRIOR ART.

Several editorial amendments have been made to the Specification. No new matter has been added.

Claims 1-5 stand rejected over the admitted prior art (APE, Specification pages 2-7 and Figs. 7 and 8) in view of Le, et al., U.S. 6,578,169.

The semiconductor test apparatus of the present invention comprises an input data generating unit for generating the input measurement data that is applied to the semiconductor test device based on input measurement conditions. There is an expected data generating unit for generating expected data for the input data under the first input measurement conditions. Further, there is a determination unit for comparing the measurement result data with the expected data, for determining whether the function of the test device is a pass or a failure, and an output of the measurement result data as determination data. There also is a data log system unit for writing in a time sequence into the log memory the associated data which includes the measurement result data, the measurement expectation data, and the determination data for a predetermined interval even after the preset writing termination conditions that terminate the writing have been satisfied. All of this is set forth in main claim 1. When the measurement indicates that the test semiconductor device is a failure, the data log system decrements the address of the log memory. An analysis of the reasons for the failure is performed and the reasons are recorded in the corresponding address of the log memory. This feature is set forth in the dependent claims.

The APE references disclose a semiconductor test device comprising a test data generation unit, an expectation data generating device, a function determination unit for determining whether the test device is a pass or a failure, a data log memory system for storing those data, including test data, expectation data, and the measurement data showing the test device is a pass or a failure. However, the APE references do not disclose the feature of the present invention which

carries out an analysis of reasons for a failure after decrementing the address of the log memory system.

Le discloses a semiconductor test system, comprising a pattern memory for producing test pattern to the semiconductor device under test (DUT), means for evaluating the output signal of the DUT, a failure data memory for storing failure data after compacting the failures data occurred in a plurality of addresses for storing failure data occurred for each group of addresses.

Le discloses a semiconductor test device, including the test pattern generation unit, a function determination unit, and log memory for storing the test result address by address. However, Le does not disclose the data log system of the present invention, in which, when a failed semiconductor device is detected, the data log system decrements the address of the log memory system for analyzing reasons for the failure and the reasons of the failure are overwritten and recorded in the decremented address. Such data is useful for use in production sites.

As should be clear, the combination of references does not meet the novel and advantageous subject matter set forth in claim 1 and its dependent claims 2-6. Therefore, these claims are patentable and should be allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Prompt and favorable action is requested.

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Respectfully submitted,

By _____
S. Peter Ludwig
Registration No.: 25,351
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 753-6237 (Fax)
Attorneys/Agents For Applicant

Attachments